

WHAT IS CLAIMED IS

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1. A semiconductor device, comprising:

a substrate;

a first multilayer interconnection structure
formed on said substrate; and

10 a second multilayer interconnection
structure formed on said first multilayer
interconnection structure,

said first multilayer interconnection
structure including a first interlayer insulation film
15 and a first interconnection layer included in said
first interlayer insulation film;

said second multilayer interconnection
structure including a second interlayer insulation
film and a second interconnection layer included in
20 said second interlayer insulation film,

said first multilayer interconnection
structure including a pillar extending from a surface
of said substrate and reaching at least said second
multilayer interconnection structure,

25 said first interconnection layer being
formed so as to avoid said pillar.

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2. The semiconductor device as claimed in
claim 1, wherein said pillar has a layered structure
identical to a layered structure of said first
interconnection layer in said first multilayer
35 interconnection structure.

3. The semiconductor device as claimed in
claim 1, wherein said pillar has a composition
different from a composition of said first
interconnection layer in said first multilayer
5 interconnection structure.

10 4. The semiconductor device as claimed in
claim 1, wherein said pillar has an edge part engaging
to a bottom surface of said second multilayer
interconnection structure.

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5. The semiconductor device as claimed in
claim 1, wherein said pillar extends further in said
20 second multilayer interconnection structure and has a
layered structure identical to a layered structure of
said second interconnection layer in a part thereof
extending in said second multilayer interconnection
structure.

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6. The semiconductor device as claimed in
30 claim 1, wherein said pillar extends further in said
second multilayer interconnection structure, and
wherein said pillar has a composition different from a
composition of said first and second interconnection
layers.

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7. The semiconductor device as claimed in claim 1, wherein an electrode pad is formed on said second multilayer interconnection structure.

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8. The semiconductor device as claimed in claim 7, wherein said pillar is formed in a region of said substrate right underneath said electrode pad in plural numbers so as to occupy at least 15% of the area of said region as a whole.

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9. The semiconductor device as claimed in claim 7, wherein there is formed an active device in a region of said substrate right underneath said electrode pad.

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10. The semiconductor device as claimed in claim 1, wherein said first interlayer insulation film has a first Young modulus and said second interlayer insulation film has a second, larger Young modulus than said first Young modulus.

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11. The semiconductor device as claimed in claim 10, wherein said first Young modulus has a value less than 30GPa and said second Young modulus has a value equal to or larger than 30GPa.

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12. The semiconductor device as claimed in claim 10, wherein said first Young modulus has a value $1/2$ or less of said second Young modulus.

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13. The semiconductor device as claimed in claim 1, wherein said pillar has a Young modulus of 30GPa or more.

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14. The semiconductor device as claimed in claim 1, wherein, in said first multilayer interconnection structure, said pillar is formed with plural numbers so as to be located at both sides of an interconnection pattern forming a part of said first interconnection layer.

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15. The semiconductor device as claimed in claim 1, wherein said pillar forms a wall extending continuously on said surface of said substrate.

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16. The semiconductor device as claimed in claim 1, wherein said pillar extends continuously along a circumference of said substrate in said first and second multilayer interconnection structures and form a guard ring.

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17. The semiconductor device as claimed in claim 1, wherein said first interlayer insulation film is formed of a porous film.

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18. The semiconductor device as claimed in claim 1, wherein said first interlayer insulation film is an organic film.

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19. The semiconductor device as claimed in claim 1, wherein said second interlayer insulation film is a CVD insulation film.

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20. The semiconductor device as claimed in claim 1, wherein said pillar is provided on a device isolation structure on said substrate

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21. The semiconductor device as claimed in claim 1, wherein said pillar is provided in plural number on said substrate, and wherein there is formed a reinforcement structure in said first multilayer interconnection structure so as to extend diagonally between said plural pillars.

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22. A multilayer interconnection structure comprising stacking of at least two interconnection layers with an intervening via-layer,

each of said interconnection layers
5 comprising an interlayer insulation film and an interconnection pattern formed in said interlayer insulation film,

said via-layer comprising a via-interlayer insulation film and a via-plug formed in said via-
10 interlayer insulation film,

said via-plug connecting said interconnection pattern in said interconnection layer located on said via-layer to said interconnection pattern in said interconnection layer located under
15 said via-layer,

said interlayer insulation film forming said via-layer having a smaller film thickness and a larger elastic modulus than any of said interlayer insulation films constituting said interconnection layers on and
20 under said via-layer.

23. The multilayer interconnection structure
25 as claimed in claim 22, wherein, in said interconnection layers on and under said via-layer, said interlayer insulation film has a film thickness of less than 300nm.

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24. The multilayer interconnection structure
35 as claimed in claim 22, wherein said interlayer insulation film constituting said via-layer has a film thickness of about 180nm.

25. A semiconductor device comprising
a substrate;
a first multilayer interconnection structure
formed on said substrate; and
5 a second multilayer interconnection
structure formed on said first multilayer
interconnection structure,
said first multilayer interconnection
structure including stacking of at least two
10 interconnection layers with an intervening via-layer,
each of said interconnection layers
comprising an interlayer insulation film and an
interconnection pattern formed in said interlayer
insulation film,
15 said via-layer comprising a via-interlayer
insulation film and a via-plug formed in said via-
interlayer insulation film,
said via-plug connecting said
interconnection pattern in said interconnection layer
20 located on said via-layer and said interconnection
pattern in said interconnection layer located under
said via-layer,
said via-interlayer insulation film
constituting said via layer having a smaller film
25 thickness and a larger elastic modulus than any of
said interlayer insulation films constituting said
interconnection layers located on and under said via-
layer,
said interconnection pattern in each
30 interconnection layer and said via-plug in each via-
layer extending, in said first interlayer insulation
film, continuously from said substrate surface through
said first multilayer interconnection structure and
forming a pillar at least reaching said second
35 multilayer interconnection structure.

26. A semiconductor device, comprising:
a substrate; and
a multilayer interconnection structure
formed on said substrate,
5 a plurality of pillars being formed in said
multilayer interconnection structure so as to reach a
surface of said substrate;
a reinforcement structure being formed in
said multilayer interconnection structure diagonally
10 among said plurality of pillars.

15 27. A semiconductor device as claimed in
claim 26, wherein there is formed another multilayer
interconnection structure on said multilayer
interconnection structure, and wherein said multilayer
interconnection structure includes an interlayer
20 insulation film having a specific dielectric constant
lower than a specific dielectric constant of an
interlayer insulation film in said another multilayer
interconnection structure provided thereon.

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28. The semiconductor device as claimed in
claim 26, wherein said reinforcement structure has a
30 layered structure identical to a layered structure of
said interconnection layer in said multilayer
interconnection structure.